

Moving forward on multiple fronts

Weebit Nano (ASX:WBT) filed several patents recently to protect the IP of its silicon oxide (SiOx) Resistive Random Access Memory (ReRAM) technology. WBT, along with its research partner Leti, filed a very valuable patent that enables the company to develop an effective programming algorithm to implement multi-level capability in any OxRAM technology. This patent will enable the implementation of multi-level programming taking into account typical physical shifts of the levels, which is common to ReRAM. After programming ReRAM cells, the ReRAM experiences a slight shift in its resistivity levels due to natural physical phenomena. Weebit's programming algorithm takes this shift into account and thus works with its "true" resistivity level and not the theoretical one. The MLC technology allows more data per unit area, leading to higher memory storage capacity and lower cost. We believe this patent provides a vital competitive edge to WBT. The other two patents filed relate to reducing the select transistor size, which will enable production of smaller, lower-cost embedded memory modules.

Cashed up for commercialisation

WBT is moving towards 'productisation' and has completed the first stage of 'stabilisation', which was focussed on making the process repeatable and consistent. This stage has improved the maturity of WBT's technology, increasing cell-to-cell uniformity, leading to higher yields (more good dies (chips) per wafer). Further, WBT recently completed a A\$9.1m capital raise with the potential for another A\$19.7m from the exercise of in-the-money options by investors. The funds will assist WBT in simultaneously supporting its growth plans for embedded and stand-alone memory modules. Management aims to sign commercial agreements by Q2 2021, which we believe will significantly drive investor interest in the stock.

Valuation of A\$1.36 per share

WBT has successfully continued its development progress on multiple fronts, such as R&D and pre-production, despite the setbacks of COVID-19. This reaffirms our confidence in management's ability and the technology's potential. We continue to expect strong upside potential for this stock and reiterate our intermediate valuation of A\$1.36 per share. Following the recent share price moves, we expect the stock to further re-rate if and when the company succeeds in closing its initial commercial agreements, expected in 1HY21.

Please see page 6 for an overview of key investment risks.

Share Price: A\$0.95

ASX: WBT

Sector: Technology Hardware & Equipment

24 September 2020

Market Cap. (A\$ m)	99.9
# shares outstanding (m)	105.1
# share fully diluted	154.0
Market Cap Ful. Dil. (A\$ m)	146.3
Free Float	100%
52-week high/low (A\$)	\$1.045 / \$0.20
Average daily volume (x1,000)	421.16
Website	www.weebit-nano.com

Source: Company, Pitt Street Research

Share price (A\$) and avg. daily volume (k, r.h.s.)



Source: Refinitiv, Pitt Street Research

Valuation metrics	
Valuation per share (A\$)	1.36

Source: Pitt Street Research

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Disclosure: Pitt Street Research directors own shares in Weebit Nano.



Table of Contents

Key patent filings boost competitive edge	3
<i>Multi-level ReRAM programming patent to improve cost competitiveness</i>	3
<i>Patents for an improved select transistor in embedded ReRAM products</i>	3
Gearing towards 'productisation'	3
Sufficiently funded to get to commercial agreements	4
High potential for emerging memory technologies	4
Conclusion and valuation	5
<i>Key investment risks</i>	5
Appendix I – SiOx ReRAM technology	7
<i>ReRAM technology: The right balance between Flash memory and DRAM</i>	7
<i>How does it work?</i>	7
<i>SiOx ReRAM's technical parameters validate its commercial use</i>	8
Appendix II – MLC technology	8
<i>MLC technology: Putting more data in the same cell is another way to increase density</i>	8
Appendix III – Analyst Certification	9
General advice warning, Disclaimer & Disclosures	10



Key patent filings boost competitive edge

Multi-level ReRAM programming patent to improve cost competitiveness

Multi-level ReRam patent will make memory production more cost-efficient vs. competition

WBT and its development partner Leti jointly filed a patent for multi-level programming in August 2020. This patent defines an efficient method to implement multi-level cell storage in ReRAM technology by taking into account resistance relaxation, typical of any ReRAM type. Any ReRAM technology or device has its own memory window (the gap between the highest resistive state to the lowest resistive state) and therefore the number of possible levels that can be inserted within this window can vary and depend on various factors. WBT's new patent calculates the specific possible levels for each memory device and in this way optimises its storage capabilities. It allows for an estimation of the adaptive number of multilevels that can be attained with a given technology.

It is a very important development for WBT as multi-level cell (MLC)¹ storage means that more than one bit per cell can be stored, leading to higher memory storage capacity without increasing the memory array size. Competitors that work without this patent, will be bereft of the advantages of optimising the number of multi-levels attainable and may find MLC implementation ineffective. Thus, we believe that this patent will not only aid WBT in staying ahead of competition but also improve its cost efficiency.

WBT's partnership with Leti has been instrumental in developing the MLC technology, with as many as five patents having been jointly filed by the two firms during the last year. The collaboration has been resilient, despite Leti's operations being temporarily shut down due to the COVID-19 pandemic.

Important to note here is that, according to the agreement with Leti, only WBT is allowed to monetise joint patents, including this latest one. I.e. only WBT can decide if it wants to license this specific IP to other industry players and competitors.

Patents for an improved select transistor in embedded ReRAM products

WBT filed two patents in July 2020 for a new select transistor that will be suitable for its SiO_x ReRAM technology. This patent uses standard Silicon-On-Insulator (SOI) low-voltage transistors, which offer superior scalability against the larger high-voltage transistors currently used in embedded ReRAM arrays.

Shrinking the selector size through the use of SOI transistors is in sync with WBT's aim of reducing the overall memory cell size. This will help produce lower-cost embedded memory modules, which will be more appealing to potential customers. Additionally, the strategy to shift to low-voltage transistors fits with industry trends as many leading fabs use SOI wafers.

Gearing towards 'productisation'

The first stage of stabilisation focussed on making the process repeatable and consistent

WBT has achieved a key milestone on the path to 'productisation' by successfully completing the first stage of the 'stabilisation' process. The goal of this phase was to establish the process as repeatable and consistent and to improve wafer yield by eliminating process issues, which affected the memory yield.

¹ Refer to Appendix II for further details on MLC technology.



The first stage improved the maturity of WBT's technology, increasing cell-to-cell uniformity, thus leading to a higher proportion of memory cells in working condition (higher yield). Moreover, the establishment of a new integration methodology will ensure that future batches maintain a solid baseline of consistent yield within the memory.

Currently, the second phase of the 'stabilisation' process is underway, with the aim to analyse and verify batch-to-batch repeatability. Notably, all the phases of process stabilisation are vital as the company is working towards transferring its technology to a production fab.

Sufficiently funded to get to commercial agreements

Recently, WBT raised ~A\$9.1m through a combination of a placement and an oversubscribed share purchase plan (SPP). It raised A\$6.6m through a two-tranche institutional placement, and A\$2.5m through the SPP – wherein the original offer size was A\$500k.

As part of the capital raising process, the company also issued 43.8m options at an exercise price of 45 cents. Given the strong share price run recently, these options are currently in-the-money and can potentially bring in A\$19.7m in fresh capital if and when exercised. The dilution would be very substantial, though, at nearly 42%.

In our view, the recent capital raise and the potential additional funds from options exercise will play a major role in enabling the company to simultaneously support the growth plans for embedded and stand-alone memory modules. The funds raised will be deployed towards WBT's commercialisation activities, including completion of the embedded memory module and transfer of technology to a production fab.

While WBT is targeting both the embedded and stand-alone memory markets in parallel, its technology for embedded applications is more mature and closer to commercialisation. Management expects to sign commercial agreements in the first half of 2021.

High potential for emerging memory technologies

The market for emerging memory technologies is forecast to reach ~US\$36bn by 2030, as per research firm Objective Analysis and Coughlin Associates. This represents an expansion of ~12x, compared with the ~\$US3bn market size in 2018.

Burgeoning applications in artificial intelligence, the Internet of Things, edge computing, Advanced Driver Assistance (ADAS) and autonomous vehicles, to name just a few, require scalable memory solutions to process dense and complex data as well as higher power efficiency.

Newer technologies, such as 3D XPoint, MRAM and ReRAM, are expected to gradually complement and, in some cases, even replace traditional storage technologies such as NOR flash and SRAM.

ReRAM is also often cited as a logical replacement in Solid State Drive (SSD) and Non-Volatile Dual In-line Memory Modules (NVDIMMs) because of its high storage density. Other benefits of ReRAM include the potential for 3D stacking, allowing a large number of memory cell layers to be coordinated and organised in one chip, fast switching for quick exchange of information and less energy use per switching cycle.

ReRAM also has the potential to replace flash memory used in mobile phones and other consumer electronics, such as cameras, smart watches etc.

In-the-money options could bring in A\$19.7m in the near term

WBT expecting to secure first commercial orders in embedded memory by Q2 2021



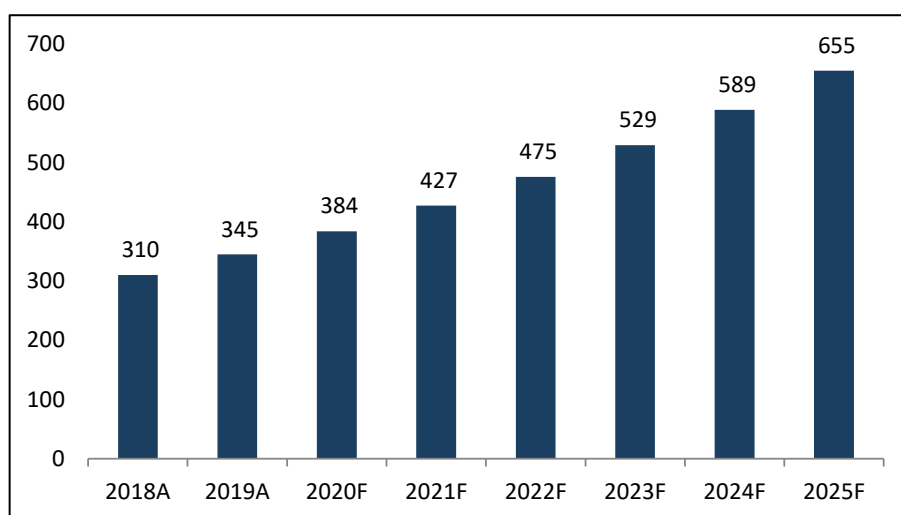
We believe potential growth for ReRAM can be substantially larger than what is currently forecast

As per research firm Market Research Future, the global ReRAM market (Figure 1) was valued at ~US\$310m in 2018 and is expected to exceed ~US\$650m by 2025, growing at a CAGR of ~10%.

However, Pitt Street Research believes that this growth rate can be substantially higher if and when truly scalable solutions, like WBT's SiOx ReRAM become commercially available, likely in 2021.

As an illustration, 3D XPoint, a non-volatile memory jointly developed by Intel and Micron, is expected to reach US\$3BN in revenues in 2023 from essentially a standing start in 2019. And this technology is not nearly as efficient as ReRAM. In other words, we believe the potential market for WBT's SiOx ReRAM is substantially larger than the US\$650m currently being forecast by Market Research Future.

Figure 1: Global ReRAM market (US\$m)



Source: Market Research Future

Conclusion and valuation

WBT successfully raised funds, which will support its commercialisation plans for both embedded and stand-alone memory programmes. Further, WBT is nearing 'productisation' and is on track, in our view, to achieve its target of signing commercial agreements by Q2 2021.

We believe the recent patent filings, particularly the one related to multi-level ReRAM programming, are a demonstration of its robust R&D capabilities and will strengthen its competitive position.

We continue to see robust upside potential and reiterate our valuation of A\$1.36 per share. We expect the share price to further re-rated if and when the company succeeds in closing initial commercial agreements.

Key investment risks

- Although WBT is getting closer to commercialisation, the company is still in the development stage of its technology, and hence there is a risk that the potential of WBT's technology may not eventuate.
- Alternative emerging memory technologies are being developed by WBT's competitors. These technologies could potentially be superior in nature and/or could be commercialized sooner than WBT's technology, which would inhibit the company's future growth.



- Although WBT now seems adequately funded for the medium term, there remains a risk that the company will need to raise further capital, for instance if its current development programs take longer than currently anticipated, resulting in dilution for existing shareholders.
- There are currently 43.8m in-the-money options overhanging the market, which have only been issued very recently (July 2020). Therefore, the holders of these options are sitting on a very substantial paper profit and may be inclined to take profits soon. If and when these options are exercised, we believe the 43.8m newly issued shares will likely be sold soon after exercise.
- COVID-19 is still posing a risk to WBT's research partner Leti in France as new lockdowns may be needed to stem the renewed increase in the rate of infections in France. Additionally, the inability to travel is posing challenges to WBT's technical and commercial people in its conversation with partners and prospects, which may slow down development and commercialisation.

Please refer to www.pittstreetresearch.com for our initiating coverage report on WBT, including more elaborate risk assessments.



Appendix I – SiOx ReRAM technology

ReRAM technology: The right balance between Flash memory and DRAM

ReRAM is a fast, cost-effective and energy-efficient non-volatile memory (NVM) technology. It can be considered a hybrid memory technology, as it is non-volatile like Flash memory and nearly as fast as DRAM, which is volatile, i.e., a DRAM cell will lose the value (1 or 0) that is stored if the power is switched off. WBT is developing SiOx ReRAM, which, in terms of performance metrics, sits right between Flash and DRAM.

How does it work?

Generally, in case of NAND Flash memory, the values of 1 and 0 are attributed on the basis of the trapped electrical charge present in the memory cell's floating gate. However, in case of a ReRAM cell, the values (1 and 0) are attributed based on the resistance level of the cell material sandwiched between the two electrodes (Figure 2). A value of 1 is attributed to a state of low resistivity, while a value of 0 is attributed to a state of high resistivity.

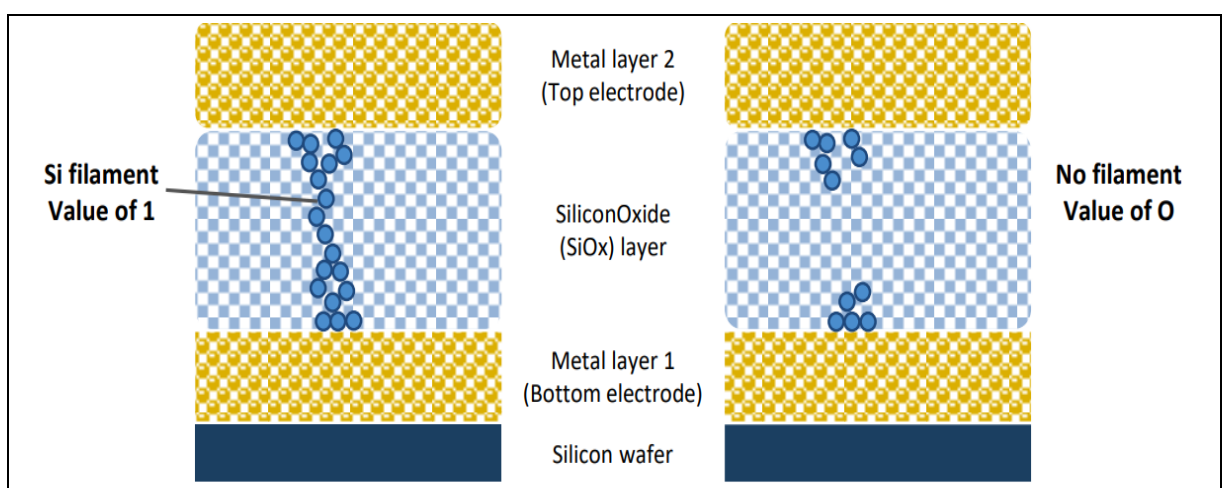
There are two ways of changing the resistance level of a ReRAM cell.

- Through interface switching, which changes the resistivity of the entire layer between the electrodes or
- By creating a filament that connects the two electrodes.

WBT uses the latter.

The technology WBT is developing is based on the forming of a conductive channel between the two metal electrodes of a ReRAM cell. These electrodes are typically made of metals, such as titanium, tungsten, aluminium or copper. The conductive channel is formed inside a non-conductive SiOx layer.

Figure 2: Cell switching by forming and breaking a silicon filament in a SiOx switching layer



Source: Pitt Street Research

SiO₂ has typically been used as an insulating component in semiconductor manufacturing. However, by applying a certain voltage to one of the electrodes, a switchable conductive pathway of silicon nanowires (filament) can be formed within the SiOx layer (Figure 2). In this high-conductivity, low-resistance state, the cell value is 1. By subsequently applying a reverse voltage

The endurance and retention levels demonstrated by WBT's technology open up many commercial opportunities

to the electrode, the filament can be broken down again, effectively switching the memory cell back to the original state of 0.

The actual filament is formed as the applied electrical voltage strips away some of the oxygen atoms in the SiOx layer, leaving the silicon atoms to cluster and form a conductive silicon pathway to the other electrode. The filament is ~5 nanometer (nm) to 7nm in diameter.

WBT uses SiOx in its ReRAM cells, a material that is well understood by the semiconductor industry and has been used in chip manufacturing for decades. We believe that the industry's familiarity with SiOx is a key factor in driving the adoption of WBT's technology among both semiconductor manufacturers and foundries.

SiOx ReRAM's technical parameters validate its commercial use

The key parameters for any non-volatile memory are retention and endurance. As demonstrated in the tests conducted by WBT's research partner Leti in May 2019, the company's ReRAM technology is at the forefront of the ReRAM market. The tests demonstrated data retention of over 10 years at 130–150°C, and endurance of a million cycles. Notably, these endurance levels are significantly higher than today's state-of-the-art Flash memory technologies.

Moreover, the retention levels that were achieved at these high temperatures have broadened the scope of potential commercial applications wherein WBT's technology can be used, including the most notable addressable market of electric vehicles.

Additionally, prospective customer XTX has independently verified and validated WBT's technology as well, providing sufficient validation of the technology, in our view.

Appendix II – MLC technology

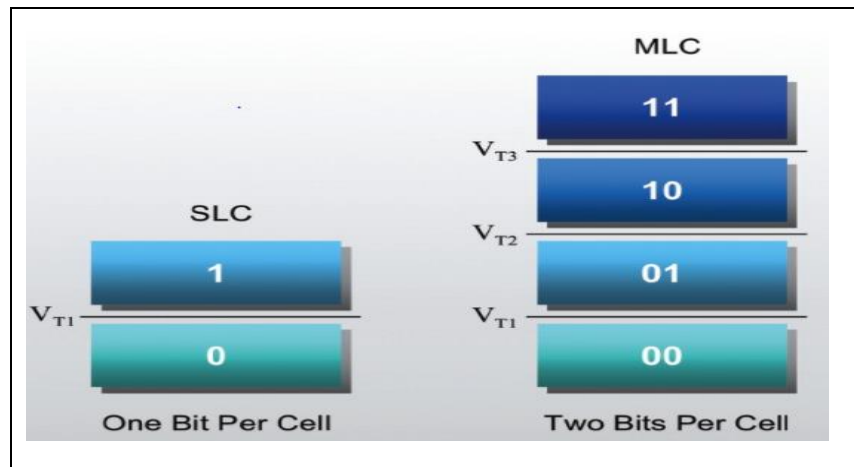
MLC technology: Putting more data in the same cell is another way to increase density

Traditionally, memory cells had two possible states, 1 and 0, and therefore could contain 1 bit of data. These cells are termed as single-level cells (SLC). However, now MLCs are available wherein the stored charge can be a variety of values and 2 bits of data can be stored in a single cell (Figure 3). MLC technology thus allows more data per unit of area to be packed onto a chip compared to SLC.

Typically, the cycling endurance and reliability required in end-user applications determine the appropriate storage technology to be used. SLCs have lower power consumption and therefore a longer lifespan compared to MLC (~100,000 cycles for SLC versus ~10,000 for MLC). Owing to higher reliability and faster speeds, SLC can be found in high-end storage applications, including data center storage. However, MLCs are less expensive to manufacture per unit of storage and this makes MLC Flash the most commonly used Flash, especially in consumer electronics such as mobile phones, cameras and tablets.



Figure 3: Relative voltage levels for SLC and MLC



Source: Pitt Street Research

Appendix III – Analyst Certification

Marc Kennis, lead analyst on this report, has been covering the Semiconductor sector as an analyst since 1997.

- Marc obtained an MSc in Economics from Tilburg University, Netherlands, in 1996 and a post graduate degree in investment analysis in 2001.
- Since 1996, he has worked for a variety of brokers and banks in the Netherlands, including ING and Rabobank, where his main focus has been on the Technology sector, including the Semiconductor sector.
- After moving to Sydney in 2014, he worked for several Sydney-based brokers before setting up TMT Analytics Pty Ltd, an issuer-sponsored equities research firm.
- In July 2016, with Stuart Roberts, Marc co-founded Pitt Street Research Pty Ltd, which provides issuer-sponsored research on ASX-listed companies across the entire market, including Technology companies.

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